What Is Claimed Is:

1. A method of driving a liquid crystal display including a liquid crystal display panel having pixels arranged in a matrix form, a gate driver for applying a scanning signal to gate lines of the liquid crystal display panel, and a data driver for supplying a picture data to data lines of the liquid crystal display panel, the method comprising the steps of:

applying a clock pulse to the gate driver;

applying first to third gate output enable signals to the gate driver; and

applying a scanning pulse to two gate lines during one period of the clock pulse.

2. The method according to claim 1, wherein the data driver supplies the picture data to the data lines when the scanning pulse is applied to a first gate line of the two gate lines, and supplies a black data to the data lines when the scanning pulse is applied to a second gate line of the two gate lines.

3. The method according to claim 1, wherein the data driver supplies a black data to the data lines when the scanning pulse is applied to a first gate line of the two gate lines, and supplies the picture data to the data lines when the scanning pulse is applied to a second gate line of the two gate lines.

4. The method according to claim 1, wherein the first gate output enable signal is applied to each of the (3i+1)th gate lines, the second gate output enable signal is applied to each of the (3i+2)th gate lines, and the third gate output enable signal is applied to each of the (3i+3)th gate lines, where i is a non-negative integer.

5. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+1)th gate line during one period of the clock signal;

applying the scanning pulse to the (3(i+k)+2)th gate line, which is thereby separated from the (3i+1)th gate line by 3k+1 gate lines, when the scanning pulse is applied to the (3i+1)th gate line, where k is a positive integer;

setting the first gate output enable signal at a high state during one half of the one period of the clock signal when the scanning pulse is applied to the (3i+1)th gate line; and

setting the second gate output enable signal at a high state during the other half of the one period of the clock signal when the scanning pulse is applied to the (3(i+k)+2)th gate line.

6. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+2)th gate line during one period of the clock signal;

applying the scanning pulse to the (3(i+k)+3)th gate line, which is thereby separated from the (3i+2)th gate line by 3k+1 gate lines, when the scanning pulse is applied to the (3i+2)th gate line, where k is a positive integer;

setting the second gate output enable signal at a high state during one half of the one period of the clock signal when the scanning pulse is applied to the (3i+2)th gate line; and

setting the third gate output enable signal at a high state during the other half of the one period of the clock signal when the scanning pulse is applied to the (3(i+k)+3)th gate line.

7. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+3)th gate line during one period of the clock signal;

applying the scanning pulse to the (3(i+k)+1)th gate line, which is thereby separated from the (3i+3)th gate line by 3k-2 gate lines, when the scanning pulse is applied to the (3i+3)th gate line, where k is a positive integer;

setting the third gate output enable signal at a high state during one half of the one period of the clock signal when the scanning pulse is applied to the (3i+3)th gate line; and

setting the first gate output enable signal at a high state during the other half of the one period of the clock signal when the scanning pulse is applied to the (3(i+k)+1)th gate line.

8. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+1)th gate line during one period of the clock signal;

applying the scanning pulse to the (3(i+k)+3)th gate line, which is thereby separated from the (3i+1)th gate line by 3k+2 gate lines, when the scanning pulse is applied to the (3i+1)th gate line, where k is a positive integer;

setting the first gate output enable signal at a high state during one half of the one period of the clock signal when the scanning pulse is applied to the (3i+1)th gate line; and

setting the third gate output enable signal at a high state during the other half of the one period of the clock signal when the scanning pulse is applied to the (3(i+k)+3)th gate line.

9. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+2)th gate line during one period of the clock signal;

applying the scanning pulse to the (3(i+k)+1)th gate line, which is thereby separated from the (3i+2)th gate line by 3k-1 gate lines, when the scanning pulse is applied to the (3i+2)th gate line, where k is a positive integer;

setting the second gate output enable signal at a high state during one half of the one period of the clock signal when the scanning pulse is applied to the (3i+2)th gate line; and

setting the first gate output enable signal at a high state during the other half of the one period of the clock signal when the scanning pulse is applied to the (3(i+k)+1)th gate line.

10. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+3)th gate line during one period of the clock signal;

applying the scanning pulse to the (3(i+k)+2)th gate line, which is thereby separated from the (3i+3)th gate line by 3k-1 gate lines, when the scanning pulse is applied to the (3i+3)th gate line, where k is a positive integer;

setting the third gate output enable signal at a high state during one half of the one period of the clock signal when the scanning pulse is applied to the (3i+3)th gate line; and

setting the second gate output enable signal at a high state during the other half of the one period of the clock signal when the scanning pulse is applied to the (3(i+k)+2)th gate line.

11. A method of driving a liquid crystal display that is driven frame by frame, comprising the steps of:

displaying a first picture on a liquid crystal display panel in the current frame;

displaying a specific pattern of picture on the liquid crystal display panel on which said picture has been displayed; and

displaying a second picture over said specific pattern of picture in the next frame.

12. The method according to claim 11, wherein the specific pattern of picture is a black picture.

13. A liquid crystal display device, comprising:

a liquid crystal display panel having a plurality of gate lines and a plurality of data lines arranged substantially in a matrix form;

a gate driver receiving a clock signal and connected to each of the plurality of gate lines, the gate driver internally and sequentially generating scanning pulses in synchronization with the clock signal, the gate driver receiving at least two gate output enable signals that respectively control different groups of the gate lines, wherein when a gate output enable signal is in an enabling state, the output of the scanning signal to the gate lines belonging to the corresponding group is enabled, and when a gate output enable signal is in a disable state, the output of the scanning signal to the gate lines belonging to the corresponding group is disabled, and wherein in one cycle of the clock signal, the gate driver generates a scanning pulse for a pair of gate lines that belong to different groups and processes the scanning pulse generated for the pair of gate lines with the corresponding gate output enable signals so as to divide the scanning pulse to two sequential pulses, the gate driver supplying one of the two sequential pulses to one of the pair of the gate lines and supplying the other one of the two sequential pulses to the other one of the pair of the gate lines; and

a data driver connected to the plurality of data lines, the data driver supplying data signals to the plurality of data lines in synchronization with the one of the two sequential pulses, the data driver further supplying a reference signal to the plurality of data lines in synchronization with the other one of the two sequential pulses.

14. The liquid crystal display device according to claim 13, wherein the gate driver receives two gate output enable signals, and the gate lines are divided into two groups of odd

numbered gate lines and even numbered gate lines, as numbered from the top to the bottom of the display panel.

15. The liquid crystal display device according to claim 14, wherein the reference signal is a black signal.

16. The liquid crystal display device according to claim 13, wherein the gate driver receives three gate output enable signals, and the gate lines are divided into three groups of (3i+1) numbered gate lines, (3i+2) numbered gate lines, and (3i+3) numbered gate lines, as numbered from the top to the bottom of the display panel, where i is a non-negative integer.

17. The liquid crystal display device according to claim 16, wherein the reference signal is a black signal.

18. A method for driving a liquid crystal display panel, comprising:

(a) selecting two gate lines that are separated by a predetermined number of gate lines;

(b) providing picture signals to a row of pixels corresponding to one of the two selected gate lines;

(c) providing a reference signal to a row of pixels corresponding to the other one of the two selected gates lines;

(d) repeating steps (a) through (c) for different pairs of gate lines so that all rows of pixels are refreshed by corresponding picture signals in one frame; and

(e) repeating steps (a) through (d) for each frame so that updated picture signals are provided to the pixels that bear the reference signal immediately prior to being updated.

19. The method according to claim 18, wherein the reference signal is the same for all rows of pixels and for each frame.

20. The method according to claim 19, wherein the reference signal is such that each pixel provided with the reference signal exhibits a black dot.

21. The method according to claim 18, wherein steps (a) through (d) are performed such that a horizontal band of pixels applied with the reference signal sweeps an entire screen of the liquid crystal display panel from the top to the bottom in each frame.

22. The method according to claim 21, wherein the horizontal band is a black band.